

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi U.S. Patent No. 5,930,271.

As per claims 1 and 3, Takahashi teaches the claimed functional block for an integrated circuit with a test data output and a control signal for test mode, with output data that changes from one value to another based on the input data (column 1 lines 23-31, column 6 lines 33-58, figure 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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Claims 2, and 4-9, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi U.S. Patent No. 5,930,271 in view of Koo et al. U.S. Patent No. 5,386,423.

As per claims 2, 4, and 5, Takahashi substantially teaches the claimed functional block for an integrated circuit with a test data output in parallel and a control signal for test mode (column 6 lines 33-58). Not explicitly disclosed is that the output signal lines are grouped and have mutually different values and that the test data will alternately change from one value to another.

However, in an analogous art, Koo et al. teach a test circuit in which outputs can be grouped and a mechanism is shown for setting adjacent latches into logically opposite states. Thus, the expected output is a string of zeroes and ones or ones and zeroes alternating accordingly (column 5 lines 1-10, column 8 lines 3-21). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have combine the testing circuits of Koo et al. and functional blocks of Takahashi. This would have been obvious to one of ordinary skill in the art because as suggested by Koo et al. (column 2 lines 52-65) in order to more easily isolate faults in a circuit.

As per claims 6-9, Takahashi and Koo et al. as combined above, substantially the claimed circuit in which Koo et al. teach a circuit which has a control line that generates and inverts the alternating zero and one signals sent to specific latches where the input to the inverter is tied to selected latches and the output to other specified latches (Koo et al. column 8 lines 7-49).

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Claims 16, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. U.S. Patent No.5,809,039 in view of Luk U.S. Patent No. 6,055,661.

As per claims 16-17, Takahashi et al. substantially teach the claimed integrated circuit divided into a plurality of functional blocks, and an output portion of each functional block is provided with a buffer circuit with a scan function which can change a function of latching data by a control signal and the test data can be entered directly to the buffer or read out of the buffer. Test patterns are generated in each functional block and diagnosis can be carried out in each functional block (column 15 lines 16-30). Not explicitly disclosed is that there is a comparison circuit which provides an output indicating a pass or fail of the test.

However, in an analogous art, Luk teaches a circuit containing a comparator which is connected to a latch controlled by a third programmable time delay. The result of the comparisons made by the comparator is latched into the latch, and pass/fail signal is generated from the latch depending on the result of the comparison made by the comparator (column 7 line 64 through column 8 line 7). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have included the comparison device of Luk in the testing circuit of Takahashi et al. This would have been obvious because as suggested by Luk, controlling the testing and

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collecting the response signals for comparison will simplify the testing process (column 3 lines 34-40).

As per claims 19 and 20, Luk teaches storing the results of the comparison in latch circuitry (column 7 line 64 through column 8 line 5).

Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi U.S. Patent No. 5,930,271 and Koo et al. U.S. Patent No. 5,386,423 in further view of Negishi U.S. Patent No. 6,119,257.

As per claims 10 and 11, Takahashi and Koo et al. as combined above substantially teach the claimed functional block of an integrated circuit in which Takahashi teaches the claimed functional block for an integrated circuit with a test data output and a control signal for test mode, with output data that changes from one value to another based on the input data (column 1 lines 23-31, column 6 lines 33-58, figure 3). And Koo et al. teach a test circuit in which outputs can be grouped and a mechanism is shown for setting adjacent latches into logically opposite states. Thus, the expected output is a string of zeroes and ones or ones and zeroes alternating accordingly (column 5 lines 1-10, column 8 lines 3-21). Not explicitly disclosed is that the system contains multiple pattern generators and a decision output circuit.

However in an analogous art Negishi teach multiple pattern generators which are selected using multiplexers, a comparison circuit for comparing test data with expected data, and an output to a memory to store the test results (figure 1, column 5 line 46 through column 6 line 30). Therefore it would have

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been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of testing a functional block as taught by Takahashi and Koo et al. with the methods of Negishi. This would have been obvious as suggested by Takahashi in order to enable independent testing of functional blocks (column 1 line 60 through column 2 line 3).

As per claims 12, and 14, Negishi teaches a method of the output being inhibited in response to a control signal (column 9 line 60 through column 10 line 4).

As per claims 13 and 15 Negishi teaches a method of inverting the signal from a pattern generator in response to a reset signal Column 8 line 66 through column 9 line 10 and column 9 lines 48-59).

Conclusion

The examiner invites applicant to call and schedule an interview prior to responding to this office action to discuss issues in the above rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117